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| **EVB ZCU216 FPGA**  **Registers Map** | | |
|  |  | C:\Users\amit_m\Desktop\LOGOs\LOGO-KRATOS_GMI_EYAL.jpg |
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| **Revision History** | | | | |
| Revision | ECN | Date | Prepared by | Description |
| 1.0 | ----- | 28.07.2022 | Yaakov Gurevich | Initial Release |
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# 

# Scope

This Specification establishes the requirements for EVB ZCU216 FPGA registers map.

# **FPGA registers**

Table: **FPGA registers memory map**

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| --- | --- | --- | --- | --- | --- |
| **Device allocated** | **Memory location** | **Data Bus Width** | **Reset Value** | **Type** | **Description** |
| FPGA Version Reg | 0x0 | 32 | Ver | Read | Bits[7:0] – ver minor  Bits[15:8] – ver major |
| FPGA Version Date Reg | 0x4 | 32 | Date | Read | DD MM YYYY |
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| Read/Write Test and RGB\_LED\_4 control | 0xC | 32 | 0x12345689 | R/W | Bit[0] – RGB\_R\_LED\_4  Bit[1] – RGB\_G\_LED\_4  Bit[2] – RGB\_B\_LED\_4  ‘0’ – OFF  ‘1’ – ON  Bit[4] – DMA\_WR\_Valid (Debug) |
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| ***RF IP Interface*** | | | | | |
|  |  |  |  |  |  |
| RF-IP TX Data Flow Control | 0x20 | 32 | 0x0003 | W/R | Bits[1:0] – TX Source Mux Select  ‘00’ – Counter  ‘01’ – Loopback (JESD\_TX <= JESD\_RX)  ‘10’ – Play-Back  ‘11’ – Pattern Gen [default] |
| TX Channels Data Mask | 0x130 | 32 | 0x00FF | W/R | Bit[0]  ‘0’ – Ch1 Transmit Null  ‘1’ – Ch1 Transmit Data [default]  Bit[1]  ‘0’ – Ch2 Transmit Null  ‘1’ – Ch2 Transmit Data [default]  Bit[2]  ‘0’ – Ch3 Transmit Null  ‘1’ – Ch3 Transmit Data [default]  Bit[3]  ‘0’ – Ch4 Transmit Null  ‘1’ – Ch4 Transmit Data [default]  Bit[4]  ‘0’ – Ch5 Transmit Null  ‘1’ – Ch5 Transmit Data [default]  Bit[5]  ‘0’ – Ch6 Transmit Null  ‘1’ – Ch6 Transmit Data [default]  Bit[6]  ‘0’ – Ch7 Transmit Null  ‘1’ – Ch7 Transmit Data [default]  Bit[7]  ‘0’ – Ch8 Transmit Null  ‘1’ – Ch8 Transmit Data [default] |
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| ***Pattern Gen Interface*** | | | | | |
| Pattern Select | 0x060 | 32 | 0x0000 | W/R | Bits[2:0] – Pattern Select  ‘000’ – Constant Zero [default]  ‘001’ – Constant DC  ‘010’ – CW Fs/16, Re/Im= -3dBFS  ‘011’ – Counter 32 bits  ‘100’ – DDS CW1  ‘101’ – DDS Two Tone (CW1+CW2)  ‘110’ – LFM Mode (Use Ch1 Pulse Width/Period Configuration for all of Channels)  ‘111’ – BPSK Mode (Use Ch1 Pulse Width/Period Configuration for all of Channels)  Bit[3] – Continue/Pulse Mode Sel  ‘1’ - Continue Mode  ‘0’ – Pulse Mode [default]; (LFM and BPSK- Pulse Mode Only) |
| Pattern Attenuator  Ch1 to Ch4  (Don’t care) | 0x064 | 32 | 0xFFFF\_FFFF | W/R | Bits[7:0] – Ch1 Attenuation Value  Bits[15:8] – Ch2 Attenuation Value  Bits[23:16]–Ch3 Attenuation Value  Bits[31:24]- Ch4 Attenuation Value  Attenuation = unsigned(Value)/2^8  0xFF – 0dB [default], CW Re/Im = -3dBFS  0x80 – -6dB  0x40 – -12dB |
| LFM Frequency Increment | 0x064 | 32 | 0x0000\_0000 | R/W | Bits[18:0]– LFM Frequency Increment (signed value)  Range [-2^18, +2^18-1]  LSB – 14.65 Hz |
| DDS CW1 Frequency,  LFM Start Frequency | 0x068 | 32 | 0x0020\_0000 | R/W | Bit[23:0]– CW1 Frequency (signed value)  Range [-Fs/2 +Fs/2]  LSB – 14.65 Hz  Before update this value write ‘000’ to reg 0x060 |
| DDS CW2 Frequency | 0x06C | 32 | 0x0040\_0000 | R/W | Bit[23:0]– CW2 Frequency (signed value)  Range [-Fs/2 +Fs/2]  LSB – 14.65 Hz  Before update this value write ‘000’ to reg 0x060 |
| Pattern Attenuator  Ch5 to Ch8  (Don’t care) | 0x070 | 32 | 0xFFFF\_FFFF | W/R | Bits[7:0] – Ch5 Attenuation Value  Bits[15:8] – Ch6 Attenuation Value  Bits[23:16]-Ch7 Attenuation Value  Bits[31:24]-Ch8 Attenuation Value  Attenuation = unsigned(Value)/2^8  0xFF – 0dB [default], CW Re/Im = -3dBFS  0x80 – -6dB  0x40 – -12dB |
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| ***Pattern Gen Output Complex Multiplier*** | | | | | |
| Complex Multiplier at Pattern Gen Ch1 output | 0x080 | 32 | 0x0000\_7FFF | W/R | Bits[15:0] – Real signed Value  Bits[31:16]- Imag signed Value  For example:   1. 0x0000\_7FFF [default] =>   Gain=0dB, Phase=+0(degree)   1. 0x4000\_4000 =>   Gain=-3dB, Phase=+45(degree)   1. 0x7FFF\_7FFF =>   Gain=+3dB, Phase=+45(degree) |
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| ***Record/Playback Interface*** | | | | | |
| Record RX Data Channel 32bit format: Bits[31:16] – Re, Bits[15:0] – Im  Record Ch0: Start Address = 0x00\_A100\_0000; Length = 512Kbyte = 128K\*32bit  Record Ch1 Start Address = 0x00\_A108\_0000; Length = 512Kbyte = 128K\*32bit  Playback Ch0: Start Address = 0x00\_A100\_0000; Length = 512Kbyte = 128K\*32bit | | | | | |
| Record Start/Busy/Ready Reg  (common for all channels) | 0x090 | 32 | 0x0000 | R/W Clear by F/W | Bit[0] – Ready/Start/Busy/Ready  ‘0’ – Record Done and Ready  ‘1’ – Start and Busy  S/W set this bit to start a new Record and F/W clear it at the end |
| Record Mux Control Reg | 0x094 | 32 | 0x0000008C | W/R | Bits[3:0] – Connect 1 of 16 ADCs to Record Ch0  Bits[7:4] – Connect 1 of 16 ADCs to Record Ch1  Bit[8] – Record Source Select  ‘0’ - Record RX data [default]  ‘1’ – Record Pattern Gen |
|  |  |  |  |  |  |
| PlayBack Control | 0x0A0 | 32 | 0x0000 | R/W | Bit[0] – PlayBack Enable  ‘0’ – Disable [default]  ‘1’ – Enable (Run) |
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| ***DMA AXIS Mux Control*** | | | | | |
| AXIS Mux Control | 0x0B0 | 32 | 0x0000 | R/W | Bits[1:0] – DMA Write Source Sel  ‘00’ – DMA Loopback  ‘01’ - Byte Counter |
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| ***I/O FPGA SPI Indirect Access*** | | | | | |
| IO FPGA SPI Status | 0x200 | 32 | 0x0001 | Read | Bit[0] – SPI Ready/Busy Status  ‘0’ - Busy  ‘1’ – Ready, Receive Data Valid |
| IO FPGA SPI Data to Transmit | 0x204 | 32 | 0x0000 | R/W | Bits[31:0] – Data to Transmit  Bit[31] – command  ‘0’ – Read access  ‘1’ – Write access  Bits[30:24] – IO FPGA Register Address  Bits[23:0] – Value to Write  (SPI starts automatically after write) |
| IO FPGA SPI Receive Data | 0x208 | 32 | 0x0000 | Read | Bits[31:24] – 0xA5 Control Symbol  Bits[23:0] – Receive Data |